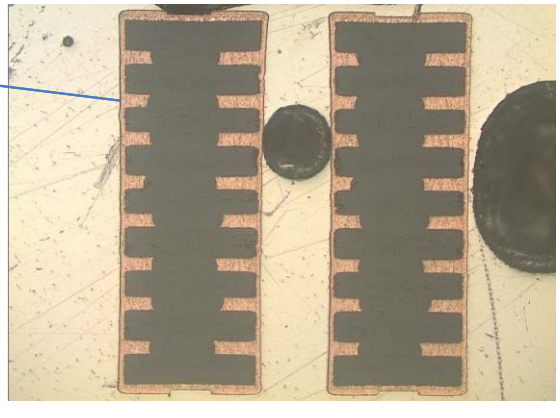
General Capability

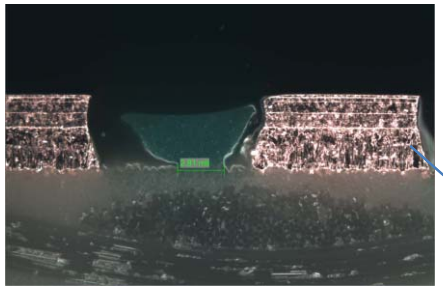
Parameters Feature		Y2024		Y2025	Y2026
		Standard	Advanced		
Line Width/Space (um)		50/50	40/40	40/40	35/35
Impedance Tolerance		10%	8%	10%	8%
Layer Count max(Traditional & HDI)		18L	20L	20L	26L
Thru hole size min (um)		100		100	75
Max Aspect Ratio (Through -hole)	0.1≦ Diam. < 0.2mm	4:1	6:1	6:1	8:1
	0.2≦ Diam.< 0.3mm	6:1	8:1	8:1	10:1
	0.3mm ≦ Diam.	8:1	10:1	10:1	12:1
Hole tolerance (um)	PTH	+/-75	+/-50	+/-50	+/-37.5
	N-PTH	+/-50	+/-25	+/-38	+/-25
Hole to Hole accuracy (um)		+/-50		+/-50	+/-38
Pattern position Tolerance (um)		+/-50		+/-50	+/-38
Routing edge to edge tolerance (um)		+/-100	+/-75	+/-100	+/-75
Min space between board to board(mm)		1.6	1.2	1.0	0.8
Finished board thickness (mm)		0.2-3.0	0.15-3.2	0.15-3.2	0.1-3.5
Board thickness tolerance (mm)	Bd thk ≥ 0.6mm	+/-10%		+/-10%	+/-8%
	Bd thk < 0.6mm	+/-0.05	+/-0.03	+/-0.05	+/-0.03

PCB Heavy copper Capability

Item		Y2024		Y2025	Y2026
		Standard	Advanced		
Copper thk max		3oz	4oz	6oz	6oz
Copper thk tolerance		+/-10%		+/-10%	+/-10%
Line Width/Space Min. (mm)	2oz	0.13 / 0.13	0.1 / 0.1	0.13 / 0.13	0.1 / 0.1
	3oz	0.2 / 0.2	0.15 / 0.15	0.2 / 0.2	0.15 / 0.15
	4oz	0.25 / 0.25	0.2 / 0.2	0.25 / 0.25	0.2 / 0.2
SMD Pad size Min. (mm)	2oz	0.2	0.18	0.2	0.18
	3oz	0.25	0.2	0.25	0.2
	4oz	0.3	0.25	0.3	0.25

IL Copper thk 3oz

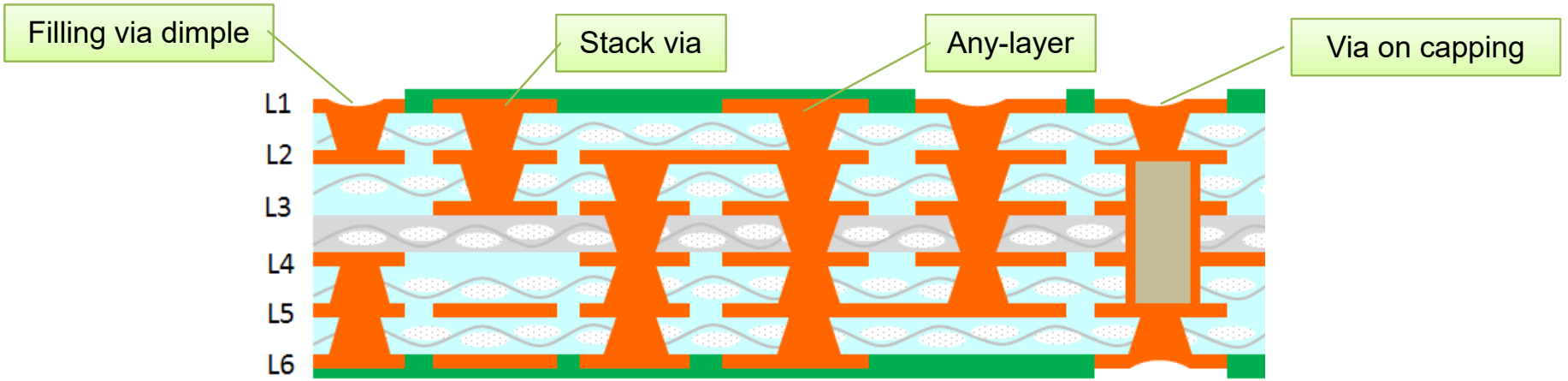




OL Copper thk 4oz

High Density Interconnect Capability

Item	Y2024		Y2025	Y2026
	Standard	Advanced		
Laser via structure	Via on Capping Stack via Any-Layer	Via on Capping Stack via Any-Layer	Via on Capping Stack via Any-Layer	Via on Capping Stack via Any-Layer
Max Layer count	12L	16L	16L	18L
Min Blind via size (mm)	0.1	0.075	0.075	0.075
Max Aspect Ratio	0.7 : 1	0.8 : 1	0.8 : 1	1 : 1
Min Blind via Capture pad (mm)	D + 0.15	D + 0.13	D + 0.13	D + 0.13
Min Blind via Target Pad (mm)	D + 0.15	D + 0.13	D + 0.13	D + 0.13
Filling via dimple value (um)	≤15	≤10	≤10	≤10

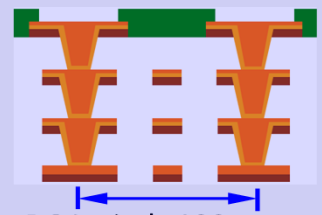
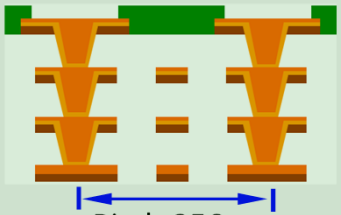
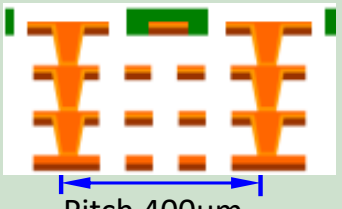
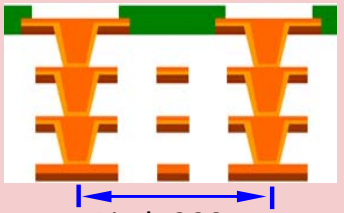
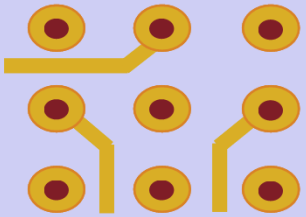
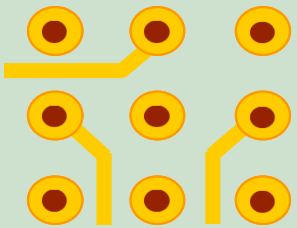
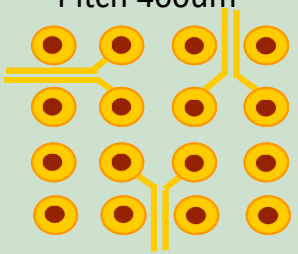
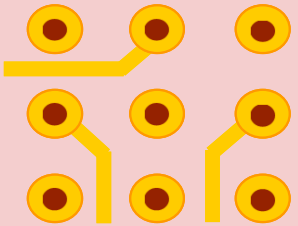


Capability Roadmap (Surface Finish)

Surface Finish	Typical Value	Supplier
OSP	0.2~0.6um 0.2~0.35um	Enthone Shikoku chemical
ENIG	Au:0.03~0.12um, Ni :2.5~5um	ATO tech
Selective ENIG	Au:0.03~0.12um, Ni :2.5~5um	ATO tech
ENEPIG	Au : 0.05~0.125um, Pd : 0.05~0.125um, Ni :5~10um	Chuang Zhi
Hard Gold	Au:0.2~1.5um , Ni : min 2.5um	Tanaka
Soft Gold	Au:0.15~0.5um , Ni : min 2.5um	Tanaka
Immersion Tin	Min 1um	Enthone
Immersion Silver	0.15~0.45um	Macdermid
HASL & Lead free HASL (OS)	1~25um	N/A

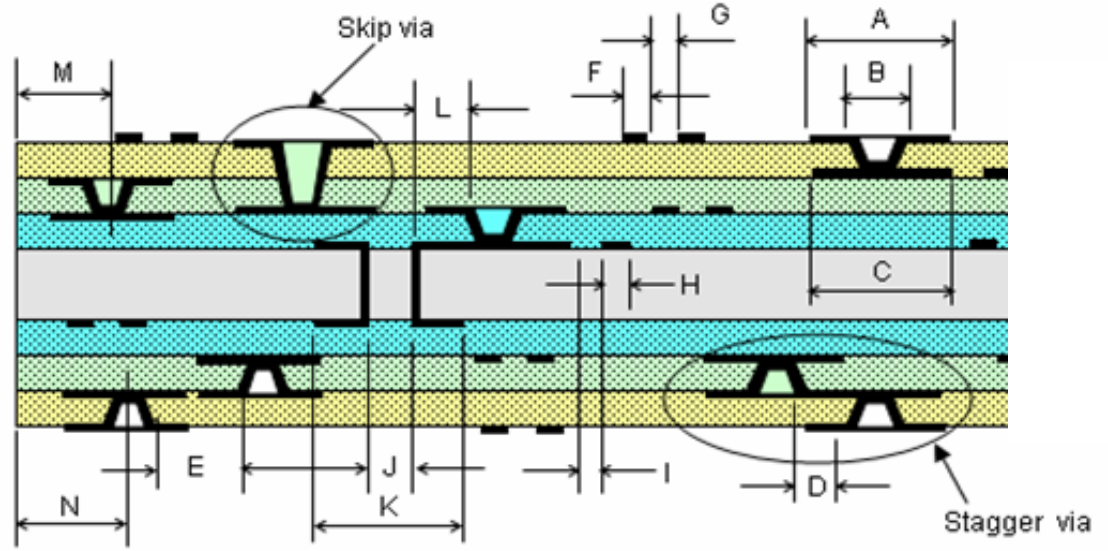
OS = Out-sourced

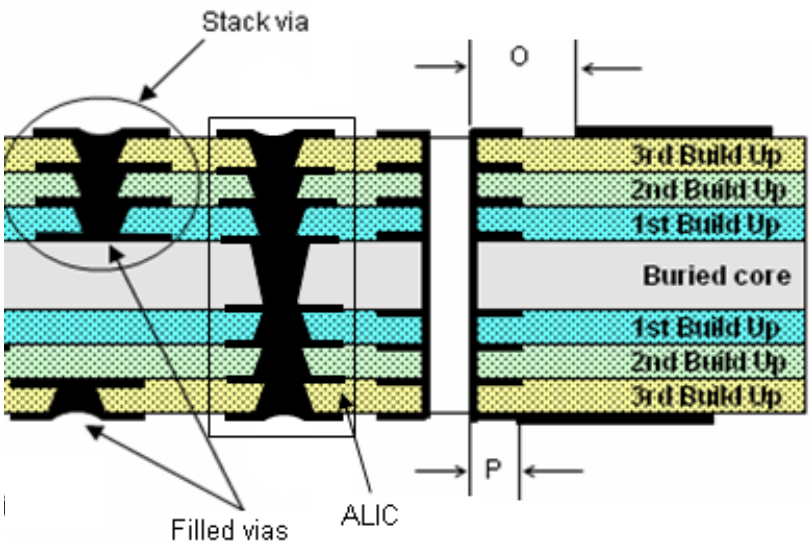
Design Guideline (HDI BGA Design Trend)

Status	MP	Prototype	Prototype	RD
HDI BGA Design Trend	 BGA pitch 400um	 Pitch 350um	 Pitch 400um	 Pitch 300um
Inner layer design	 IL: 0.4mm pitch cross 1 track	 OL: 0.35mm pitch IL: 0.35mm pitch	 OL: 0.4mm pitch cross 1 track IL: 0.4mm pitch cross 2 track	 IL: 0.3mm pitch cross 1 track

Item			Design	Design	Design	Design
Inner layer	Laser via		100um	100um	75um	75um
	Line width/ Space		50/50um	40/40umm	40/40um	45/40um
	Laser pad		D+150um	D+130um	D+125	D+100
Outer layer	Line width/Space		---	---	50/75um	----
	SM define	SM open size	220um	200um	---	180um
		SM Coverage	50um	40um	---	35um
	Copper define	Pad size	220um	---	200um	175um
		SM clearance	50um	---	37.5um	25um
		SM Dam	75um	---	125um	75um

HDI Design Guideline (I)

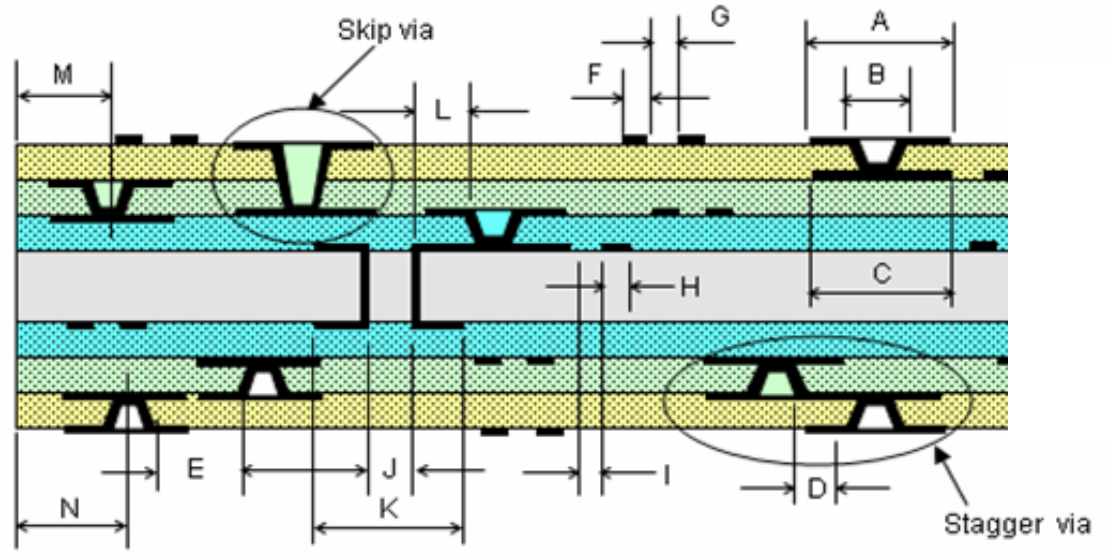


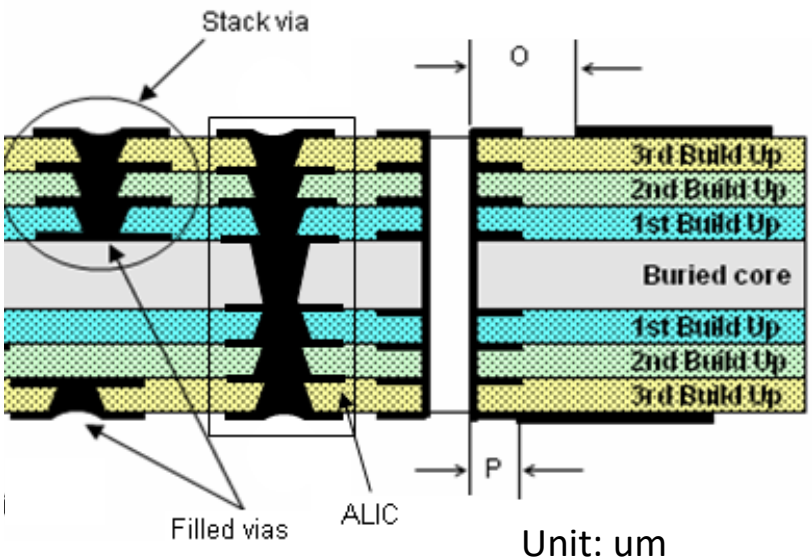


Unit: um

Symbol	Description	Standard	Advance
A	Laser via capture pad size	250	200
B	Laser via hole size	100	75
C	Laser via land pad size	250	220
D	Minimum spacing between laser hole edge to laser hole edge (Same Net)	100	100
E	Minimum spacing between laser hole edge to laser hole edge (Different Net)	250	200
F	Minimum line width on outer layer	60	50
G	Minimum line spacing on outer layer	60	50
H	Minimum line width on inner layer	60	50

HDI Design Guideline (II)

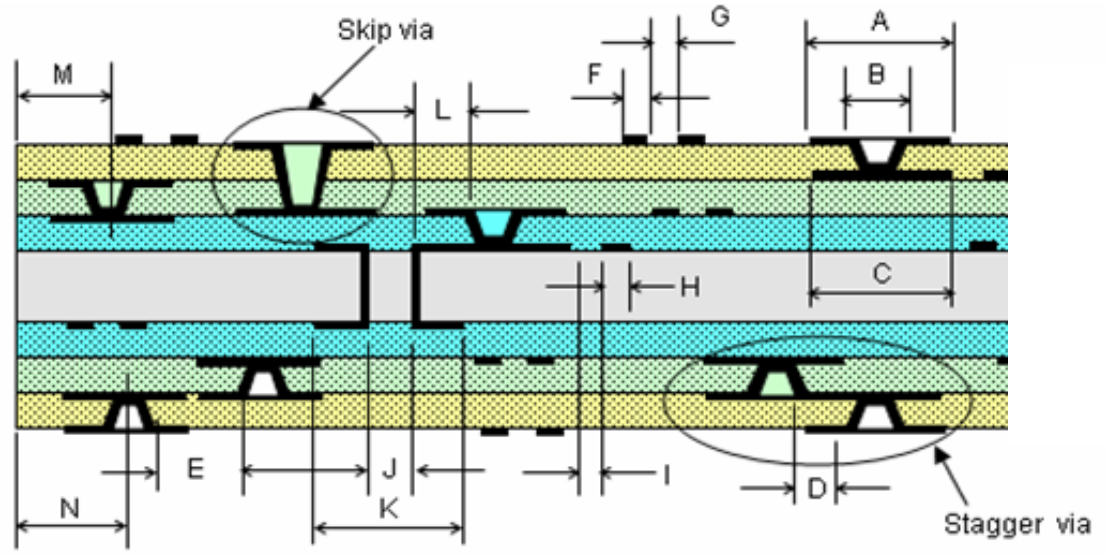


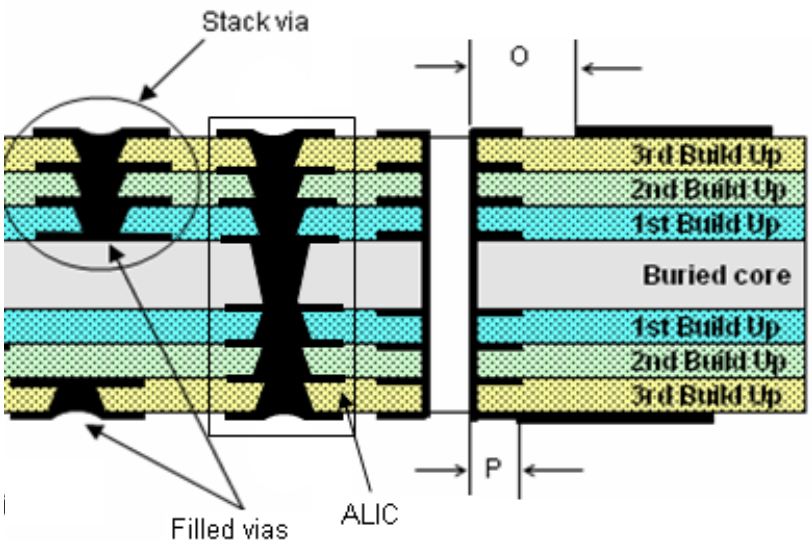


Unit: um

Symbol	Description	Standard	Advance
I	Minimum line spacing on core layer	60	50
J	Minimum buried via drill size	200	200
K	Minimum buried via pad size	D+200	D+150
L	Minimum spacing between laser hole edge to buried drill hole edge (Same Net)	150	125
	Minimum spacing between laser hole edge to buried drill hole edge (Different Net)	300	220
M	Minimum spacing between laser hole center to board edge (Inner layer)	400	350
N	Minimum spacing between laser hole center to board edge (Outer layer) Stamped/Routed edge	350	350

HDI Design Guideline (III)

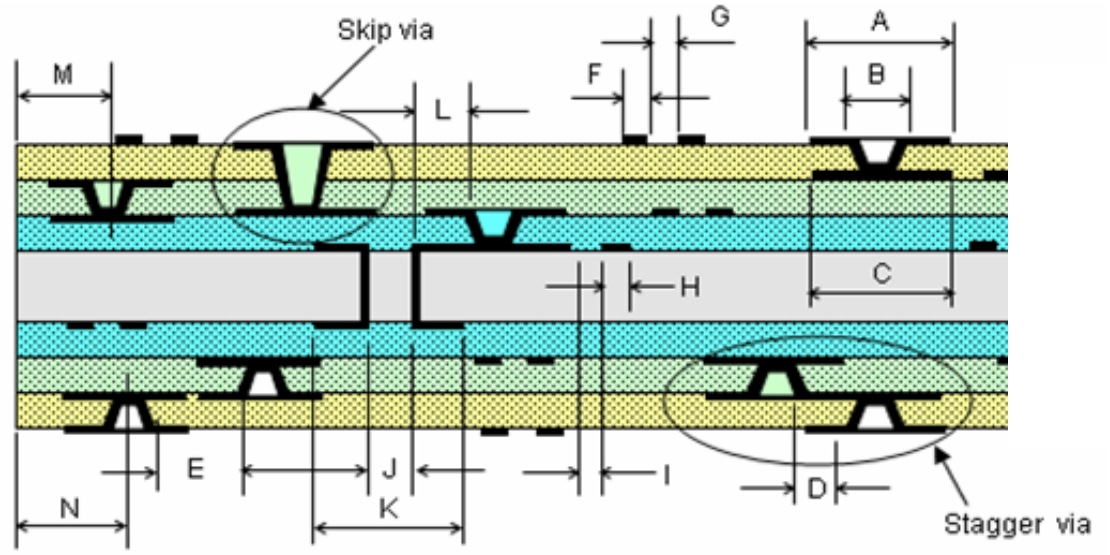


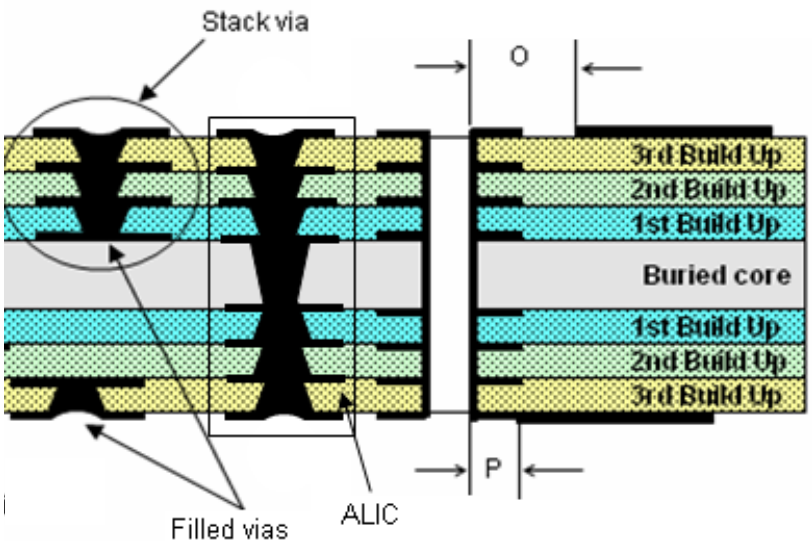


Unit: um

Symbol	Description	Standard	Advance
O	Minimum spacing between through VIA hole edge to PADs (Outer layer) (Different Net)	200	180
-	Minimum layers build up thickness	60	0.8 : 1
-	Maximum layers build up thickness	80	80
-	Maximum Aspect ratio (dielectric thickness/laser hole size)	0.7 : 1	0.8 : 1
-	Minimum CCL thickness	75	50

HDI Design Guideline (IV)

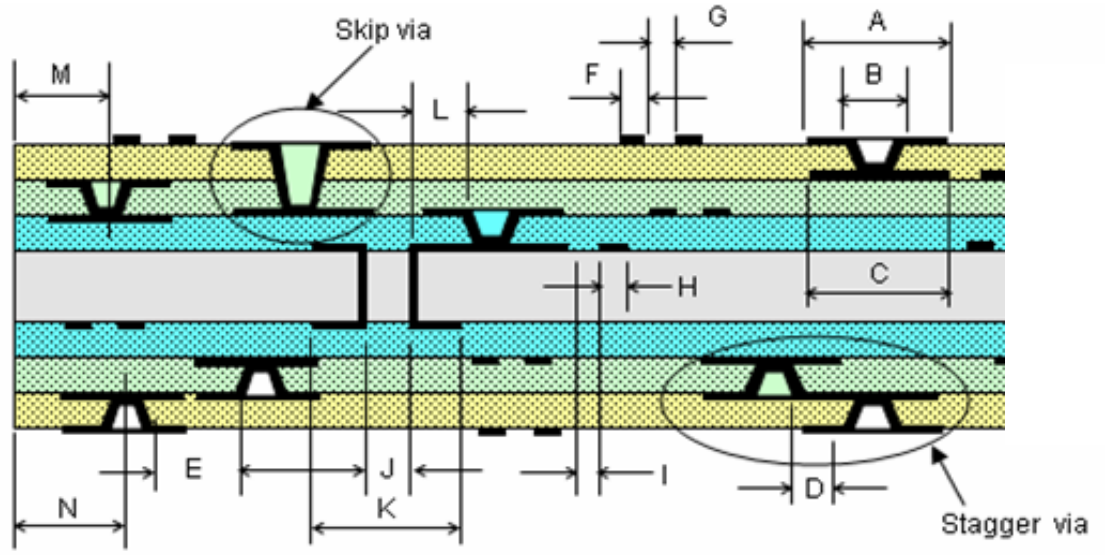


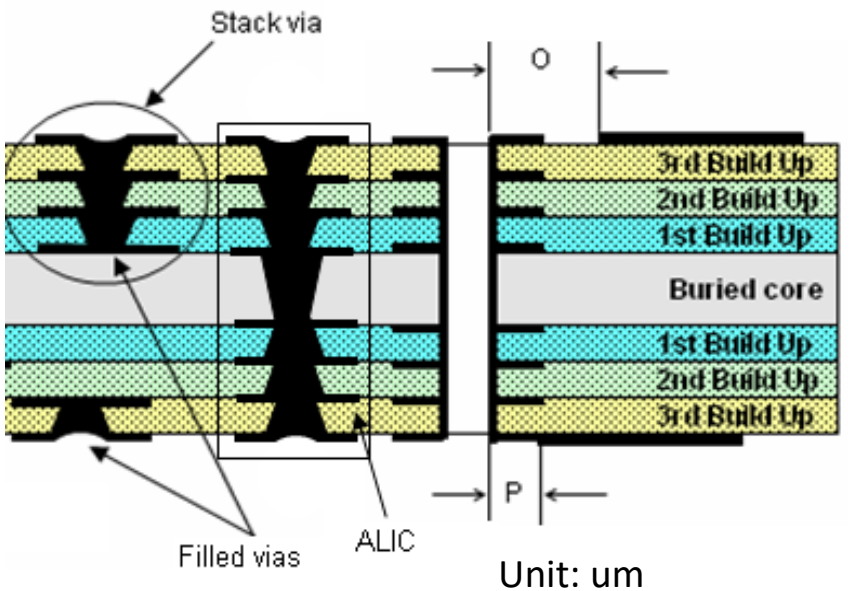


Unit: um

Symbol	Description	Standard	Advance
-	Minimum Cu thickness on outer layers (After plating)	25	20 (LW/LS＜75/75)
-	Minimum Cu thickness on inner layers (After plating)	20	18 (LW/LS≤60/60)
-	Minimum Cu thickness in Laser via holes	10	12
-	Minimum Cu thickness in buried via holes	15	18
-	Minimum Cu thickness in through holes	18 (LW/LS＞75/75)	20 (LW/LS＞75//75) 18 (LW/LS:60/60~75/75) 15 (LW/LS≤60/60)

HDI Design Guideline (V)





Unit: um

Symbol	Description	Standard	Advance
-	Stack via	4step	7step
-	Stagger via	4step	7step
-	ALIC (**A**ny **L**ayer **I**nter **C**onnect)	12L	14~16L
-	Maximum Layer count (1+N+1)	18	20
-	Maximum Layer count (2+N+2)	18	20
-	Maximum Layer count (3+N+3)	18	20
-	Maximum Layer count (4+N+4)	18	20